

# Synchronization of Active Power Filter under Distorted Grid Conditions

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## ABSTRACT

Advancement in technology has resulted in increased use of electrical energy. The trend of using energy-saving appliances is also increased considerably. Harmonic currents have been increased in power systems due to the large-scale use of nonlinear loads. Shunt Active Power Filter (SAPF) is the most widely used technique for the compensation of current harmonics. Under adverse grid conditions performance of SAPF is affected badly. In this paper, a modified synchronous reference frame theory is proposed for current reference generation by incorporating an advanced phase-locked loop technique for the estimation of frequency and phase. The proposed approach results in an accurate extraction of reference current in the presence of various grid disturbances. Matlab/Simulink environment is used for evaluating the performance. The results achieved show excellent performance of the proposed technique in terms of reducing harmonics distortion and dynamic response. The total harmonics distortion of the compensated source current is reduced to a value well within the limits of the IEEE-519 standard.

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## 1. Introduction

Power quality improvement has become an important issue to be considered in recent times. The non-linear loads connected to the power system introduce current harmonics, thus reducing the power quality to a great extent [1]. Harmonics is considered as the major issue among various power quality problems [2][3][4]. Harmonics are generally defined as integer multiples of fundamental frequency [5][6]. Harmonics in the power system are increasing rapidly due to the large-scale use of power electronics equipment [7][8]. The negative effects of harmonics include tripping of circuit breakers, overheating of cables and transformers, failure of capacitors, increase in resistive losses or voltage stress, and power factor reduction [9][10][11]. A shunt active power filter (SAPF) is considered the best solution for the mitigation of current harmonics [12]. It has two main parts, a current reference generation, and a current injection at the point of common coupling. The block diagram of SAPF connected to a three-phase source driving a three-phase non-linear load is shown in Fig. 1.

Reference current generation is a significant part of the active power filter. It is actually equal in magnitude and opposite in phase to the harmonics current. The reference current injected at the point of common coupling will make the source current sinusoidal. Existing

techniques used for reference current generation have been sub divided into time domain and frequency domain. Time-domain techniques include Instantaneous Reactive Power Theory and Synchronous Reference Frame theory, while frequency-domain techniques consist of Discrete Fourier Transform and wavelet theory.

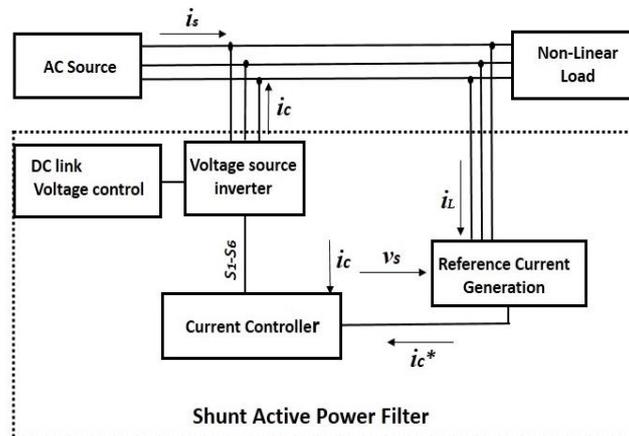


Fig. 1. Block diagram of SAPF

In [13], comparison of five techniques used for generating the reference, the current was presented. The performance of IRP theory, SRF theory, and UPF was not satisfactory under distorted grid conditions. The author proved that the PHC technique was very effective under all conditions. A harmonic detection scheme based on the Goertzel algorithm was proposed in [14]. The technique was effective in terms of using less computation time and fewer stored coefficients. In [15], a computationally efficient and robust technique based on discrete Fourier transform was proposed for this purpose. This technique was simulated under non-ideal conditions, and its robustness and computational efficiency were verified by experimental results. In [16], two theories were compared for the generation of reference current, and it was concluded that SRF theory was more efficient in reducing harmonic distortion as compared to the p-q theory. In [17], six different techniques were evaluated for current reference generation, and the perfect harmonic compensation technique was found best among all. Three techniques, including p-q theory, SRF theory, and DFT, have been evaluated in the presence of different non-linear loads [18][19]. For balanced load, the p-q theory gives better results, but for un-balanced conditions, DFT shows better performance. In [20], self-tuning filter algorithm is implemented to get the reference current. The key benefit of this technique is its simplicity and efficiency in non-ideal voltage conditions. In [21], the instantaneous power theory was observed under the effects of supply voltage harmonics. It was concluded that in the presence of distorted supply, the compensating current contained a disturbing component due to which this method was not able to extract the reference current. Davood Yazdani in [22] proposed an adaptive notch filtering approach to generate the reference current. This method was able to extract the current harmonic components efficiently. A comparison of IRP theory and Fryze current computation technique was presented in [23]. Yacine Terrechi in [24] proposed a matrix pencil-based reference current generation technique. The author proved the effectiveness of the method having a good dynamic performance under unbalanced and distorted voltage. The voltage phase was also accurately estimated by the proposed method.

The synchronization of grid-connected power converters is one of the important issues to be solved in industrial and power applications [25]. Synchronization is the process of extracting the information about frequency and phase of the fundamental frequency positive sequence component of the grid voltage. The phase information of the grid voltage is needed to obtain the reference of the current delivered by the power electronics converter [26]. This

infers that the quality of the injected power highly depends on the accuracy of phase information.

Synchronous reference frame theory has been widely used for current reference generation. This theory uses the conventional phase-locked loop method to provide frequency and phase information for the co-ordinate transformation blocks. This approach works well under normal grid conditions, but the presence of grid disturbances affects the performance of PLL, which results in inaccurate extraction of the reference current.

A phase-locked loop is commonly used for the synchronization of grid-connected power converters [27]. Between several types of PLL, synchronous reference frame PLL (SRF-PLL) established on PI controller is perhaps the most frequently used technique due to its simple implementation and structure [28]. Many researchers have worked on SRF-PLL for the estimation of grid phase and prove its accuracy if the electric grid does not contain harmonics and is balanced. On the other hand, if the grid voltage contains harmonic components, the SRF-PLL shows an inaccurate estimation of phase [29][30][31][32][33][34][35].

In [36][37][38], moving average filter (MAF) is used in the control loop of PLL. This approach is proved to be effective under adverse grid conditions. However, the open-loop bandwidth of PLL is drastically reduced after incorporating MAF into its structure, giving rise to slower dynamic response. In [39], PLL techniques, including MAF-PLL, were compared for synchronization of the active power filter. In this case, the performance was satisfactory in filtering different orders of harmonics, but the speed of response was slow.

In order to improve the dynamic response, many techniques have been proposed by researchers. Delayed signal cancellation PLL (DSC-PLL) has been proposed in recent times [40]. In this method, the signal is canceled by adding it to its time-delayed opposite phase version [41][42]. DSC-PLL shows good capability in filtering only certain orders of harmonics. Nevertheless, in order to eliminate all orders of harmonics, five DSC blocks are necessary to be cascaded. In [43], an improved DSC-PLL including a phase lead compensator is proposed that shows good filtering capability and fast dynamic response. In [44], delayed signal cancellation is investigated for harmonic extraction under an adverse grid by adopting a generalized trigonometric function. In [45], a fractional-order sliding-mode control scheme based on a two-hidden-layer recurrent neural network (THLRNN) is proposed for a single-phase shunt active power filter. A novel switching pulse generation methodology based on adaptive fuzzy hysteresis current controlled hybrid shunt active power filter (A-F-HCC-HSAPF) is presented in [46]. In [47], a single-phase cascaded H-bridge multilevel active power filter directly accessed to the 27.5-kV traction network is proposed to eliminate the low-frequency oscillation phenomenon in the vehicle-grid system of high-speed railways. Reference [48] presents a finite set model predictive control (FS-MPC) applied to the shunt active power filters (SAPF) based on three-phase inverters connected in parallel sharing the same DC-link.

### 1.1. Work Methodology

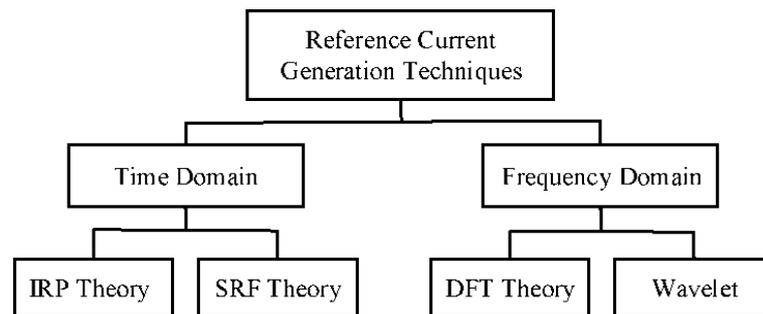
The techniques used for active power filter control have been reviewed and their shortcomings have been identified. Matlab/Simulink has been used to evaluate the proposed technique and results have been evaluated by comparing the results with the already published work.

This paper contributes by presenting a modified SRF theory for reference current generation. Modification is made by using an advanced PLL instead of SRF-PLL for estimation of frequency and phase. Phase locked loop techniques have been evaluated under various grid disturbances like frequency drift, phase angle jump and presence of dc offset. The best evaluated PLL technique is applied to provide information of frequency and phase for the SRF theory. This modified theory is used to generate the reference current and SAPF is evaluated under adverse grid conditions.

This paper is organized such that [section 2](#) describes reference current generation technique. In [section 3](#), an overview of phase-locked loop techniques is presented. Results are given in [section 4](#), and [Section 5](#) concludes the paper.

## 2. Reference Current Generation

Reference current generation is a significant part of the active power filter. The reference current is actually equal in magnitude and opposite in phase to the harmonics current. Thus injection of this current at the PCC will result in the cancellation of harmonics current and a sinusoidal current waveform. The reference current generation techniques are generally classified as time domain and frequency domain, as shown in [Fig. 2](#). In this paper, the d-q theory is implemented for current reference generation due to its simplicity and accuracy.

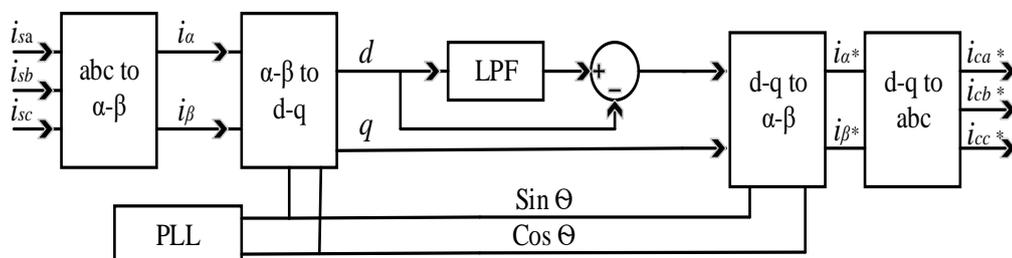


**Fig. 2.** Types of Reference Current Generation Techniques

### 2.1. Synchronous Reference Frame Theory

It is another time-domain method for the generation of the reference current. This theory is commonly used due to its simplicity and easy implementation. The real currents in the synchronous reference frame are obtained by performing co-ordinate transformation. This method also requires a PLL to estimate the frequency and phase of the grid voltage, thus synchronizing it with the ac mains voltage. This technique is also known as the d-q theory. The fundamental component is extracted by using a low-pass filter. The performance of this method is best under normal grid conditions, but the presence of grid disturbances affects the accuracy of PLL circuitry used by this theory. Thus the reference current obtained is also not accurate. This theory also requires a lot of voltage and current transducers.

[Fig. 3](#) shows the block diagram of SRF theory. The  $\sin\theta$  and  $\cos\theta$  represent the synchronized reference signals. Four transformation blocks are used to get the reference current. Harmonics current can be obtained by doing transformation from  $abc$  stationary reference frame to rotating  $dq$  frame. Finally, the reference current is obtained by transforming back from  $dq$  to  $abc$ .



**Fig. 3.** Block diagram of SRF theory

The currents in  $\alpha\beta 0$  co-ordinates are obtained using (1).

$$\begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ 1 & -1/2 & 1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (1)$$

In this paper, a three-phase three-wire balanced system is considered. Thus the zero sequence component is ignored, as shown in (2).

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & 1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (2)$$

The d-q frame is obtained by the angle  $\theta$  with respect to the  $abc$  frame, and the angle is obtained using a PLL.

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \sin(\theta) & -\cos(\theta) \\ \cos(\theta) & \sin(\theta) \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \quad (3)$$

The current represented in  $dq$  frame contains both AC component as well as DC component as shown in (4) and (5).

$$i_d = \tilde{i}_d + \bar{i}_d \quad (4)$$

$$i_q = \tilde{i}_q + \bar{i}_q \quad (5)$$

The AC component contains a harmonic component and is eliminated by using a low pass filter so that the output of the above equation, which is the DC component is harmonic free. This harmonic free signal in  $dq$  rotating frame is converted back into  $abc$  stationary frame ( $i_a^*$ ,  $i_b^*$  and  $i_c^*$ ) by doing inverse transformation from  $dq$  to  $\alpha\beta$  and then from  $\alpha\beta$  to  $abc$  as shown below.

$$\begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} = \begin{bmatrix} \sin(\theta) & -\cos(\theta) \\ \cos(\theta) & \sin(\theta) \end{bmatrix}^{-1} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \quad (6)$$

$$\begin{bmatrix} i_a^* \\ i_b^* \\ i_c^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ 1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} \quad (7)$$

### 3. Phase-Locked Loop

In order to accurately determine the reference current, precise information of the voltage phase and frequency is required. It is easier to estimate frequency and phase under normal grid conditions, but it becomes a challenge under adverse grid conditions. For this purpose, phase-locked loop (PLL) techniques are used. Synchronous reference frame PLL (SRF-PLL) is the standard PLL used in three-phase applications, but under distorted grid conditions, it cannot perform well. In this section, an overview of a more advanced PLL technique is presented.

#### 3.1. Cascaded Delayed Signal Cancellation PLL

This theory is very likely used for the generation of reference current in order to improve the performance of PLL in adverse grid conditions, initially delayed signal cancellation (DSC) technique is used. The positive and negative sequence components of the grid voltage are detached according to the voltage vector in a stationary ( $\alpha\beta$ ) reference frame, and the voltage vector is delayed by a quarter of a cycle.

The CDSC technique can be applied for the estimation of frequency and phase under the effects of odd and even harmonics, triplen harmonics, and interharmonics. The basic idea of the delayed signal cancellation method is to cancel a signal by adding the signal to its time-

delayed opposite phase version of the signal. Generally, two signals of opposite phase when added, cancel each other. This method can be used to create a harmonic free input signal. Therefore, it is necessary to create a 180 degrees' phase shift through time delay in the harmonics of the input signal to cancel them. Further, adding the input signal and the time-delayed harmonics signal cancels the harmonics present in the signal, and the input signal is free from harmonics. In the process, two signals of the same magnitude are added, therefore to maintain the DC gain of the input signal, the resultant signal is divided by 2. The general expression of the single block of the DSC operator is shown in (8).

$$y(t) = \frac{1}{2} [x(t) + x\left(t - \frac{T}{m}\right)] \tag{8}$$

Where  $m$  is the delay factor,  $x(t)$  is the input, and  $y(t)$  is the output of the block. The single DSC module can eliminate parts of harmonic meanwhile do not amplify others simultaneously. The block diagram of a single DSC module operating on the voltages in  $\alpha\beta$  frame is shown in Fig. 4.

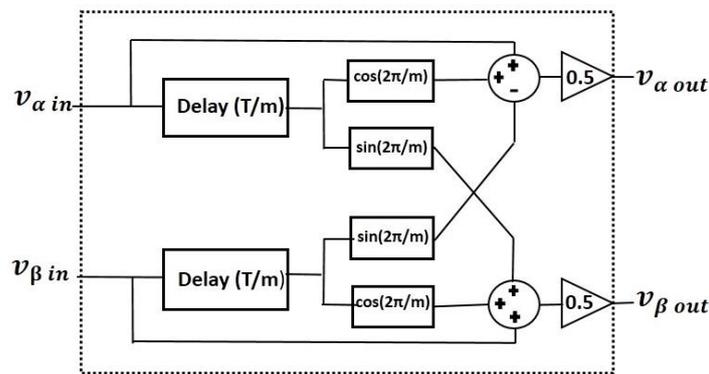


Fig. 4. Single DSC Module

The DSC block can be expressed mathematically by (9).

$$v_{\alpha\beta out} = \frac{1}{2} [v_{\alpha\beta in}(t) + e^{\frac{j2\pi}{m}} v_{\alpha\beta in}\left(t - \frac{T}{m}\right)] \tag{9}$$

The Laplace transform of (9) results in (10).

$$v_{\alpha\beta out}(s) = \frac{1}{2} [1 + e^{\frac{j2\pi}{m}} e^{-\frac{T}{m}s}] v_{\alpha\beta in}(s) \tag{10}$$

Where

$$\frac{1}{2} \left[ 1 + e^{\frac{j2\pi}{m}} e^{-\frac{T}{m}s} \right] = \alpha\beta DSC_m(s) \tag{11}$$

Substituting  $s = j\omega$  in (11) and applying mathematical simplifications to determine the magnitude and phase angle as shown in (12).

$$\alpha\beta DSC_m(j\omega) = \left| \cos\left(\frac{\omega T}{2m} - \frac{\pi}{m}\right) \right| \angle \left(\frac{\omega T}{2m} - \frac{\pi}{m}\right) \tag{12}$$

The frequency response of the DSC operator for  $m=4$  and  $T=0.02s$  is shown in Fig. 5. The  $\alpha\beta DSC_4$  allows the positive sequence components to pass through and blocks the negative sequence component and reject harmonics of the order  $h = 4k-1$  ( $k=1, 2, 3, \dots$ ). However, harmonics of the order  $h=4k+1$  are not eliminated.

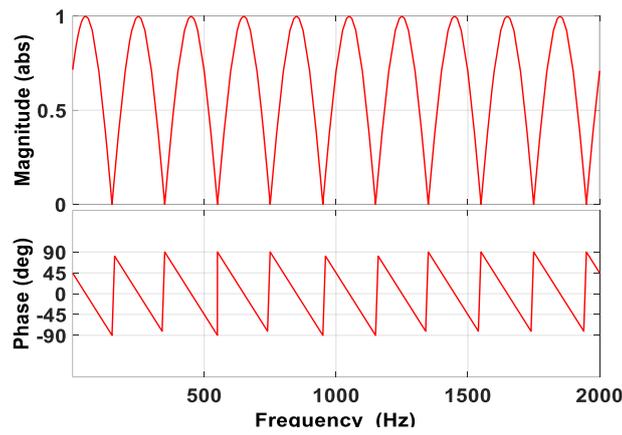


Fig. 5. Frequency response of DSC4 operator

The DSC operator can be cascaded to cancel a wide range of harmonics. The cascaded delayed signal cancellation (CDSC) filter is very flexible in adjusting the delay time by selecting the number of DSC blocks in series.

The  $k$  cascaded  $\alpha\beta$ DSC operator with delay factors  $m_1, m_2, m_3, \dots, m_k$  can be approximated by

$$\alpha\beta\text{DSC}_{m_1, m_2, m_3, \dots, m_k}(s) = \prod_{i=1}^k \alpha\beta\text{DSC}_{m_i}(s) \tag{13}$$

In our case, single DSC module with delay factor  $m = 2, 4, 8, 16,$  and  $32,$  respectively, are cascaded as shown in Fig. 6. The resultant operator  $\alpha\beta\text{DSC}_{2,4,8,16,32}$  is described in  $s$ -domain as:

$$\alpha\beta\text{DSC}_{2,4,8,16,32}(s) = \prod_{m=2,4,8,16,32} \alpha\beta\text{DSC}_m(s) \tag{14}$$

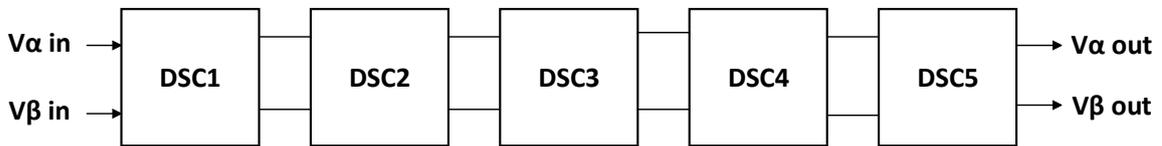


Fig. 6. Cascaded Module

The CDSC-PLL control block is shown in Fig. 7, which comprises a transformation block, a delay operator, a PI controller, and an integrator. The delayed signal cancellation is applied to  $\alpha\beta$  co-ordinates of the voltage signals. After the implementation of CDSC block, the voltage signals are again transformed from  $\alpha\beta$  co-ordinates to  $d-q$  co-ordinates.

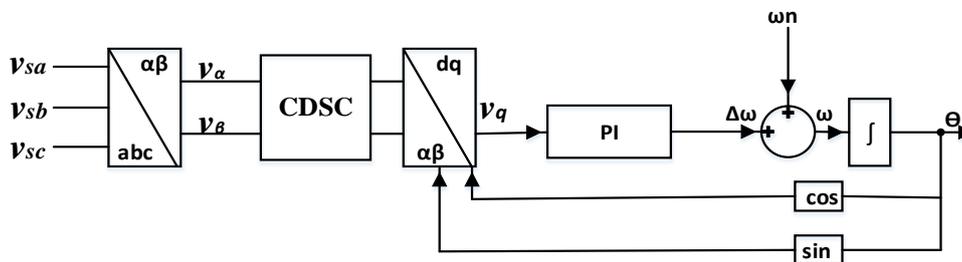


Fig. 7. Block diagram of CDSC-PLL

#### 4. Simulation Results

In this section, simulation results are obtained by adopting CDSC-PLL for generating the synchronism signals for SRF theory used for reference current generation. SAPF has been

evaluated under various grid disturbances like frequency drift, phase angle jump, and presence of dc offset.

Two load cases are considered for simulation, and their parameters are shown in Table 1. For the first case, the RL load is connected to the source, and the resultant current waveform is shown in Fig. 8. The reference current generated using the modified SRF theory is shown in Fig. 9.

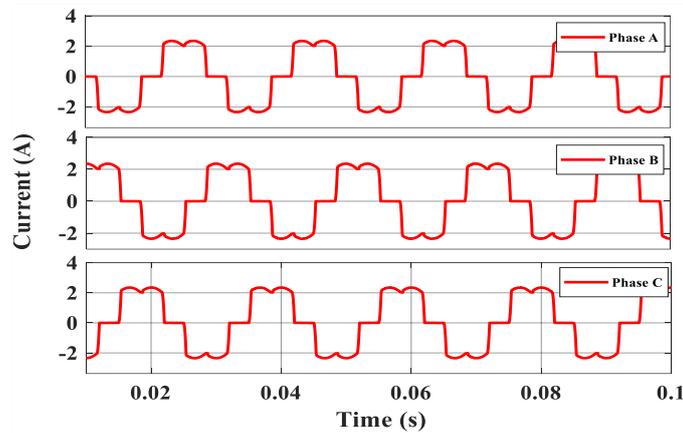


Fig. 8. Load Current (case1)

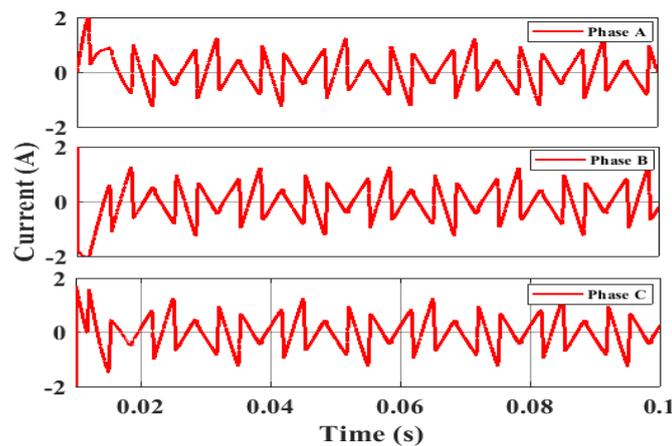


Fig. 9. Reference Current (case1)

In the second case, RLC load is used for simulation, and load current waveform is shown in Fig. 10. The reference current for RLC load is again extracted using the proposed technique and is shown in Fig. 11. Finally, the reference current generated is injected at the point of common coupling using the hysteresis current controller. Thus a sinusoidal current waveform is achieved. Shunt active power filter is investigated under different grid disturbances, and the results are shown in Table 1 and Table 2.

Table 1. Load parameters

Load	Description	% THD before compensation
<b>Non-linear load</b>	3-phase Diode Rectifier	
<b>Load 1</b>	50 $\Omega$ , 10 mH	27.45
<b>Load 2</b>	50 $\Omega$ , 100 $\mu$ F	30.61

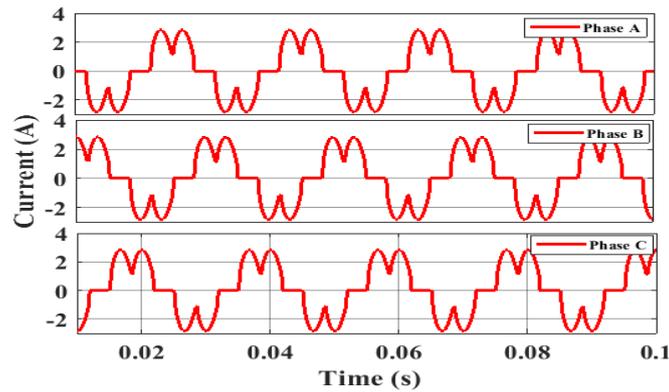


Fig. 10. Load Current (case2)

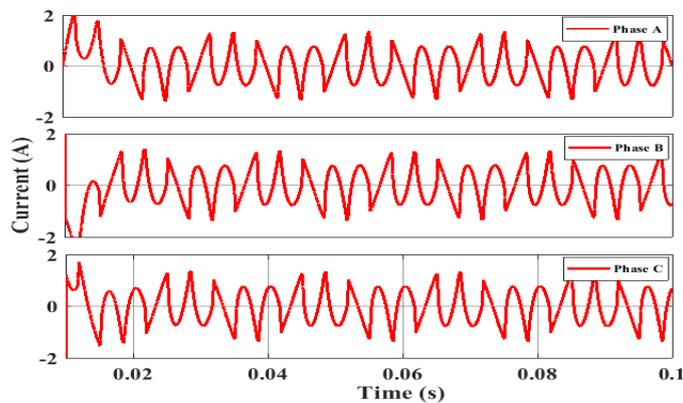


Fig. 11. Reference Current (case2)

Table 2. Summary of results

Test Case	Compensated % THD with synchronization	
	Load 1	Load 2
Normal Grid condition	1.47	1.65
Frequency jump of +3 Hz	1.70	1.84
Presence of DC offset	3.13	4.84
Phase angle jump of +10°	2.92	2.97

## 5. Conclusion

In this paper, the shunt active power filter has been evaluated under distorted grid conditions. The importance of synchronization feature for active power filter under such conditions has been realized. In order to get superior performance under adverse grid conditions, a modified synchronous reference frame theory for reference current generation is being proposed. Modification is made by using cascaded delayed signal cancellation PLL for getting the synchronism signals instead of the conventional PLL technique. The proposed approach has been verified for good performance under the effects of frequency drift, phase angle jump, and dc offset. The robustness of the active power filter is also increased with the proposed control strategy.

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**Conflict of Interest:** I being the corresponding author, states that there is no conflict of interest.

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